CMP Challenges and Opportunities for 3D Silicon Photonics

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1/ Introduction

Artificial intelligence (AI) demand grows exponentially and requires significant computational power, which leads to high energy consumption. In this context, power-efficient, low-latency interconnects are critical for large language models.

This invited talk first introduces STMicroelectronics and CEA-LETI. It then describes the emerging photonics market and the limitations of electrical links. For several years, electrical links are no longer able to support the required data rates and have been replaced by optical interconnects in data centers.

2/ ST Microelectronics

STMicroelectronics is a silicon photonic devices world leader manufacturer. This technology integrates all transceiver functions that are needed for transmission and reception and is based on 300 mm complementary metal-oxide-semiconductor (CMOS) manufacturing capabilities.

The talk also presents the STMicroelectronics roadmap for silicon photonics research, development, and industrialization. In 2013, STMicroelectronics introduced photonic devices on a 300 mm platform (PIC25G), achieving 25 GBd per lane and 100 Gbit/s with four fibers. This year, STMicroelectronics introduces the next silicon photonics platform, PIC100G, which supports 200 Gbps per lane.

This new technology requires many chemical-mechanical polishing (CMP) steps and presents several technical challenges, including planarization, design rule management (DRM), and process risks in relation to device functionality which will be exposed during this talk. In our process integration we integrate different SiN and Si waveguides which require dedicated CMP as described in Figure1. All these challenges lead to strong collaboration with CEA-LETI especially for pad/slurry benchmarking.

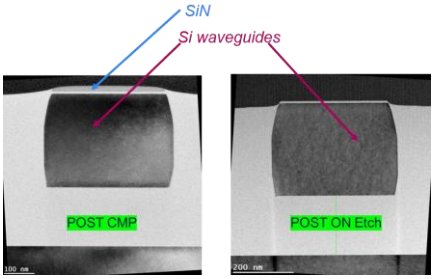

Figure 1: CMP Oxide stop on Nitride for Si waveguide integration

3/ CEA-LETI

The CEA-LETI is developing the key technological building blocks required for novel 3D photonics architectures. One major improvement for photonic devices would be the integration of III-V materials to enhance modulator performance or to integrate lasers directly in the chip. As these materials are costly and currently limited to 4-inch or 6-inch wafer sizes, one approach investigated at LETI is wafer reconstruction enabled by die bonding, thinning, encapsulation, and planarization, as illustrated in Figure 2.

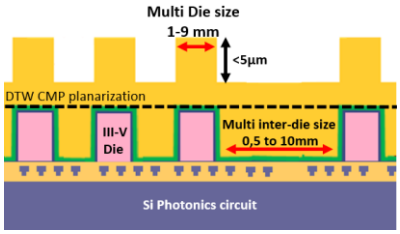

Figure 2: Wafer reconstruction with III-V bonded dies for advanced photonics devices

Moreover, 3D heterogeneous die stacking could open the new era of device architecture by enabling direct connections between photonic and logic or memory chips, thereby significantly increasing data transfer and processing capabilities, as illustrated in Figure 3.

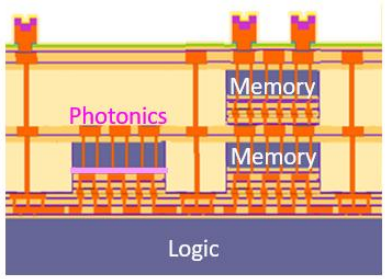

Figure 3: 3D heterogenous die stacking architecture

To achieve this, Die To Wafer CMP is a key process that needs to be developed and established. It must be capable of planarizing dies with heights ranging from 3 to 15 µm and with die densities varying from ultra-low (3 %) to ultra-high (up to 75 %), while maintaining a final surface flatness below 100–200 nm. This work will provide valuable insights into the polishing challenges investigated at CEA-LETI and the technological barriers that need to be overcome for DTW to enable next generation photonics manufacturing standard.