October 20 (Tue.), 2026

[Oral 03] CMP for Advanced Packaging/3D Integration (I)

13:55-15:20

International Conference Hall (B1F)

● Session Chair: Bradley Wood (SPS International, USA)

13:55-14:20 [Oral 03-1]	**[Invited]** Challenges for PRE-AND Post Wafer Bonding CMP Applications Wei-Tsu Tseng, Mevan Dissanayake, Toshi Kasai, Jim Kelly, Yasir Sulehria, and Matthew Shoudy (IBM Semiconductor Research, USA)
14:20-14:40 [Oral 03-2]	Panel-Level CMP Integration for Cu RDLs in Fine-Pitch Fan-Out Panel-Level Packaging Eungchul Kim, Suhyeon Jeon (Samsung Electronics Co., Ltd, Korea), Yuya Otsuka, Takehiro Yamazaki, Shinya Watanabe (DSRJ, Japan), Yongrae Kim, Dongjoon Oh, Juil Choi, and Minwoo Rhee (Samsung Electronics Co., Ltd, Korea)
14:40-15:00 [Oral 03-3]	Process Optimization of Bulk Si Thinning for Advanced Logic Architecturea Lea Di Donato, Bart Kenens, and Kevin Vandersmissen (imec, Belgium)
15:00-15:20 [Oral 03-4]	Sub-10nm Cu/SiO_2 Dishing Control for 3D Heterogeneous Integration Jinhyoung Lee, Junmin Ahn, and Taesung Kim (Sungkyunkwan Univ., Korea)