CMP at the Inflection Point: Enabling Sub-2nm and Beyond

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For three decades, scaling was driven largely by geometric shrinking. That approach is now reaching its limits. As the industry crosses into the sub-2nm regime, progress increasingly depends not on dimensions alone, but on architecture. Gate-All-Around FET, Forksheet, 3D-stacked FET, backside power delivery networks, buried power rails and wafer bonding are reshaping how devices are built, replacing planar simplicity with steep three-dimensional topography, ultra-thin films, and stacked active layers. At the intersection of these shifts sits Chemical Mechanical Planarization (CMP). Once a finishing step, CMP has become a gating enabler—now responsible for near-perfect planarity, atomic-scale surface control, and zero-defectivity on structures that did not exist a generation ago.

CMP has faced such crossroads before. From replacing LOCOS with shallow trench isolation, to tungsten contacts, copper damascene and low-k, to high-k metal gate and FinFET, each architectural leap forced a step-change in slurry chemistry, pad design, and endpoint detection—and each time, CMP absorbed the challenge and redefined its limits of dishing, erosion, and local uniformity. The sub-2nm inflection sits on this same continuum, but the demands are different in kind, not degree: where nanometer-scale particles become critical defects and removal must be controlled atom by atom, the margin for error effectively disappears.

The road ahead reframes familiar problems as new opportunities. Next-generation slurries and pads must deliver selective, residue-free removal under ultra-low pressure across heterogeneous metal and dielectric stacks. Three-dimensional metrology and real-time endpoint detection must see into buried gates, stacked devices, and backside structures. Post-CMP topography must tighten further, since residual step height now directly translates into device parameter variation at sub-2nm dimensions. And in bonding- and thinning-based integration, CMP can no longer be tuned after the fact—it must be co-designed with device and BEOL architecture from the outset. Meeting these demands will draw on AI-driven autonomous process control, real-time metrology, and increasingly, sustainable green chemistry. Drawing on more than two decades of CMP development across DRAM, Flash, and advanced Logic at Samsung Electronics, this keynote argues that how we answer these challenges will help define the trajectory of semiconductor scaling itself.